CLAIMS

1. A semiconductor device, comprising:

a plurality of landing pads formed in the semiconductor device, the landing pads being sized and shaped to be used with bonding pads;

a plurality of bonding pads formed over a first portion of the landing pads; and

a power supply line formed over a second portion of the landing pads.

2. The semiconductor device of claim 1, wherein the bonding pads are formed in a first direction on the semiconductor device and the power supply line is formed in a second direction.

3. The semiconductor device of claim 2, wherein the first and second directions are perpendicular.

4. The semiconductor device of claim 2, wherein the first and second directions are different.

5. The semiconductor device of claim 1, wherein the power supply line is a power voltage supply line.

6. The semiconductor device of claim 1, wherein the power supply line is a ground line.

7. The semiconductor device of claim 1, further comprising a second power supply line formed over the second portion of the landing pads.

8. The semiconductor device of claim 7, wherein one of the first and second power supply lines is one of a power voltage line and a ground line.

9. The semiconductor device of claim 8, wherein the other of the first and second power supply lines is the other of the power voltage line and the ground line.

10. The semiconductor device of claim 1, wherein each of the landing pads comprises a conductive layer.

11. The semiconductor device of claim 1, wherein each of the landing pads comprises a metal layer.

12. The semiconductor device of claim 1, wherein each of the landing pads comprises a polysilicon layer.

13. The semiconductor device of claim 1, wherein each of the landing pads comprises a gate polysilicon layer, a plate polysilicon layer and a metal layer.

14. The semiconductor device of claim 1, wherein the semiconductor device is a memory circuit.

15. The semiconductor device of claim 1, wherein the semiconductor device comprises a plurality of memory blocks defining a center region of the semiconductor device between memory blocks and an edge region at an edge of the memory blocks.

16. The semiconductor device of claim 15, wherein the landing pads are formed in both the center region and the edge region.

17. The semiconductor device of claim 1, wherein one of the bonding pads and the power line is formed in one of the center region and the edge region, and the other of the bonding pads and the power line is formed in the other of the center region and the edge region.

18. The semiconductor device of claim 1, wherein the device can be used in one of a board on chip (BOC) configuration and a multichip package (MCP) configuration.

19. A semiconductor device, comprising:

a plurality of circuit blocks defining a center region between circuit blocks and an edge region at an edge of the circuit blocks;

a first plurality of landing pads formed in the center region and a second plurality of landing pads formed in the edge region, the landing pads being sized and shaped to be used with bonding pads;

a plurality of bonding pads formed over one of (i) the first plurality of landing pads and (ii) the second plurality of landing pads; and

a power supply line formed over the other of the first plurality of landing pads and the second plurality of landing pads.

20. The semiconductor device of claim 19, wherein the circuit blocks are memory blocks.

21. The semiconductor device of claim 19, wherein the bonding pads are formed in the center region, and the power supply line is formed in the edge region.

22. The semiconductor device of claim 19, wherein the power supply line is formed in the center region, and the bonding pads are formed in the edge region.

23. The semiconductor device of claim 19, wherein the bonding pads are formed in a first direction on the semiconductor device and the power supply line is formed in a second direction.

24. The semiconductor device of claim 19, wherein the power supply line is a power voltage supply line.

25. The semiconductor device of claim 19, wherein the power supply line is a ground line.

26. The semiconductor device of claim 19, further comprising a second power supply line formed over the other of the first plurality of landing pads and the second plurality of landing pads.

27. The semiconductor device of claim 26, wherein one of the first and second power supply lines is one of a power voltage line and a ground line.

28. The semiconductor device of claim 27, wherein the other of the first and second power supply lines in the other of the power voltage line and the ground line.

29. The semiconductor device of claim 19, wherein each of the landing pads comprises a conductive layer.

30. The semiconductor device of claim 19, wherein each of the landing pads comprises a metal layer.

31. The semiconductor device of claim 19, wherein each of the landing pads comprises a polysilicon layer.

32. The semiconductor device of claim 19, wherein each of the landing pads comprises a gate polysilicon layer, a plate polysilicon layer and a metal layer.

33. The semiconductor device of claim 19, wherein the device can be used in one of a board on chip (BOC) configuration and a multichip package (MCP) configuration.

34. A method of manufacturing a semiconductor device, comprising:

forming a plurality of landing pads in the semiconductor device, the landing pads being sized and shaped to be used with bonding pads;

forming a plurality of bonding pads over a first portion of the landing pads; and

forming a power supply line over a second portion of the landing pads.

35. The method of claim 34, wherein the bonding pads are formed in a first direction on the semiconductor device and the power supply line is formed in a second direction.

36. The method of claim 34, further comprising forming a second power supply line over the second portion of the landing pads.

37. The method of claim 34, wherein the semiconductor device is a memory circuit.

38. The method of claim 34, further comprising forming a plurality of memory blocks defining a center region of the semiconductor device between memory blocks and an edge region at an edge of the memory blocks.

39 The method of claim 38, wherein the landing pads are formed in both the center region and the edge region.

40. The method of claim 34, wherein one of the bonding pads and the power line is formed in one of the center region and the edge region, and the other of the bonding pads and the power line is formed in the other of the center region and the edge region.

41. The method of claim 34, wherein the device can be used in one of a board on chip (BOC) configuration and a multichip package (MCP) configuration.

42. A method of manufacturing a semiconductor device, comprising:

forming a plurality of circuit blocks defining a center region between circuit blocks and an edge region at an edge of the circuit blocks;

forming a first plurality of landing pads in the center region and a second plurality of landing pads in the edge region, the landing pads being sized and shaped to be used with bonding pads;

forming a plurality of bonding pads over one of the first plurality of landing pads and the second plurality of landing pads; and

forming a power supply line over the other of the first plurality of landing pads and the second plurality of landing pads.

43. The method of claim 42, wherein the circuit blocks are memory blocks.

44. The method of claim 42, wherein the bonding pads are formed in the center region, and the power supply line is formed in the edge region.

45. The method of claim 42, wherein the power supply line is formed in the center region, and the bonding pads are formed in the edge region.

46. The method of claim 42, wherein the bonding pads are formed in a first direction on the semiconductor memory device and the power supply line is formed in a second direction.

47. The method of claim 42, further comprising forming a second power supply line over the other of the first plurality of landing pads and the second plurality of landing pads.

48. The method of claim 47, wherein one of the first and second power supply lines is one of a power voltage line and a ground line.